Anurag Singh

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Education

Chaitanya Bharathi Institute of Technology (CBIT) — Hyderabad, India
Bachelor of Engineering in Electronics & Communication; GPA: 9.28 (Upto VI sem) — *2023 – 2027*

Kendriya Vidyalaya — Hyderabad, India
Class XII (CBSE-PCM); Score: 96% (100/100 in Chemistry) — *2021 – 2023*

Technical Skills

Core Electronics: VLSI Design, Verilog HDL, Computer Architecture, FPGA (Spartan-7), Embedded Systems, Circuit Simulation
Programming: Python, C++, MATLAB, JavaScript, HTML/CSS
Tools & Platforms: Xilinx Vivado, Cadence Virtuoso, PSpice, Proteus, Git/GitHub

Internship Experience

Indian Institute of Technology (IIT) Kharagpur — Kharagpur, India
NPTEL Summer Intern, SWAN Lab — *Jun 2026 – Aug 2026*

- Selected for a 12-week in-person summer internship under the guidance of Prof. Sudip Misra.
- Focusing on advanced System Design and contributing to hardware-oriented research initiatives.

Chips to Startup (C2S) Program — Hyderabad, India
Project Intern (VLSI & FPGA) — *Jun 2025 – July 2025*

- Selected for the government-initiative program focused on semiconductor design flows and FPGA prototyping.
- Gained hands-on experience in RTL design, simulation, and hardware validation using Xilinx tools.
- Successfully delivered the **Delta-Sigma Modulator** project (detailed in Projects section) as part of the cohort.

Infosys Springboard — Remote
Project Intern (AI/ML) — *Oct 2024 – Dec 2024*

- Developed a multilingual Speech-to-Speech translation system supporting 12 languages using LangChain and Azure OpenAI.

Projects

INT8 Matrix Multiplication Engine & AI Accelerator | *Verilog, Cadence Virtuoso* — Mar 2026 – Present

- Designed and implemented an INT8 Matrix Multiplication Engine tailored for AI acceleration, utilizing Verilog HDL to code systolic arrays for highly efficient parallel computation.
- Executed the complete RTL-to-GDSII physical design flow, navigating synthesis, floorplanning, placement, and routing to optimize latency, throughput and PPA metrics.

FPGA-Based Delta-Sigma Modulator | *Verilog, Xilinx Vivado, Spartan-7* — Oct 2024

- Engineered a first-order Digital-to-Analog Converter (DAC) entirely in the digital domain using synchronous Verilog logic.
- Implemented core DSP architecture including digital integrators and 1-bit quantizers to achieve **Noise Shaping** and **Oversampling** at 100 MHz.
- Utilized Pulse Density Modulation (PDM) to emulate analog voltage levels without external filtering components, validating results via hardware LED persistence.

Certifications & Achievements

Samsung Semiconductor Fellowship: Selected for ISWDP Cohort 4 (IISc Bangalore).

NPTEL Elite Gold (Top 1%): System Design through Verilog; Micro & Nano Sensors; Google Cloud Computing.

NPTEL Elite Silver: VLSI Design Flow: RTL to GDS.